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DESIGN OF LOW VOLTAGE AND LOW POWER LEVEL SHIFTER BY USING 180nm CMOS TECHNOLOGY

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ABSTRACT

This brief presents a fast and power-efficient voltage levelshifting circuit capable of converting extremely low levels of input voltages into high output voltage levels. The efficiency of the proposed circuit is due to the fact that not only the strength of the pull-up device is significantly reduced when the pull-down device is pulling down the output node, but the strength of the pull-down device is also increased using a low-power auxiliary circuit.Simulation results of the proposed circuit in a 0.18-µm technology demonstrate a static power dissipation of 0.3 nW, and a propagation delay of 30 ns for input frequency of 1 MHz, low supply voltage level of VDDL =0.4 V, and high supply voltage level of VDDH =1.8 V.

I. INTRODUCTION

One of the most effective ways to reduce dynamic and short-circuit power consumption of digital circuits is lowering the value of the power supply voltage . On the other hand, reducing the supply voltage increases the propagation delay of the circuits. Moreover, less headroom in analog circuits decreases signal swings and therefore increases the sensitivity to noise. Hence, in moderate-speed mixedsignal circuits or in digital circuits where different parts operate at different speeds, dual-supply architectures are introduced in which a low voltage (i.e., VDDL) is supplied for the blocks on the noncritical paths while a high supply voltage (i.e., VDDH) is applied to the analog and the high-speed digital blocks.

In a system with dual supply voltages, level-shifting circuits are needed to convert the lower logic levels into the higher ones to provide correct voltage levels for the next digital blocks. In order to alleviate the degradation of the overall performance of the circuit, the required level shifters must be

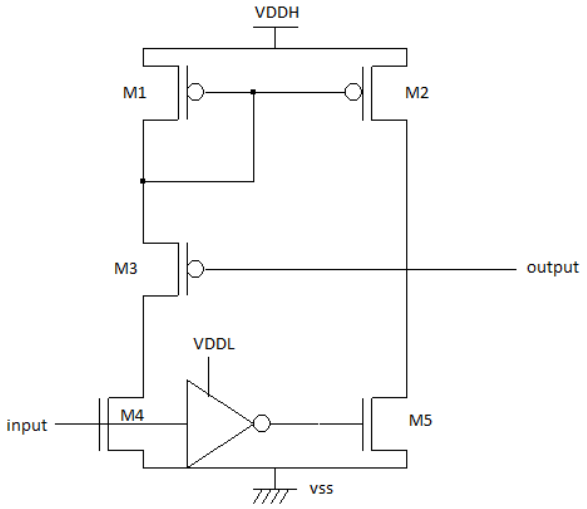
designed with minimum propagation delay, power consumption, and silicon area. In addition, in order to have more power saving in the low-supply blocks, the employed level shifters must be able to convert the extremely low values of VDDL to even lower than the threshold voltage of the input transistors. Hence, in this brief, a fast and power-efficient voltage level shifter is proposed, which is able to convert extremely low values of the input voltages.

II. LITERATURE SURVEY

In order to decrease the static power consumption, a dynamic current generator, which turns on only during the transition times. The structure shown in Fig. 1 employs a dynamic current generator implemented by MP3. In this circuit, when the input signal IN goes from "Low" to "High," MN2 turns off and MN1 turns on and pulls the node QB down. Since the node OUT had been "Low" (before the transition), during the time interval in which OUT is not corresponding to the logic level of the input signal IN,MP3 will be turned on. Therefore, a transition current flows through MN1,MP3, and MP1. This current is mirrored to MP2 (i.e., IP2) leading to pull the node OUT up. Finally, when OUT is pulled up to VDDH,MP3 is turned off and therefore no static current flows through MN1,MP3, and MP1. On the other hand, when the input signal IN is changed from "High" to "Low," MN1 turns off and MN2 turns on trying to pull the node OUT down.

III EXISTING LEVEL SHIFTER WITH DYNAMIC CURRENT MIRROR

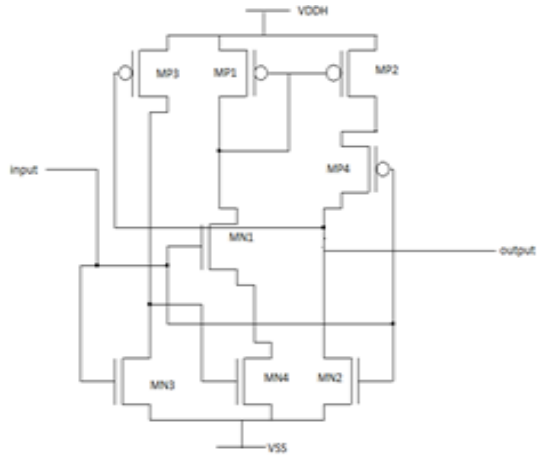
The architecture of the existing system is mentioned in figure



As the node OUT is gradually pulled down, MP3 is turned on trying to charge the node QB, which is already discharged to the ground, meaning that a transition current (i.e., IP1) flows through MP1 and MP3 to charge node QB. This current is mirrored to MP2 (i.e., IP2) and therefore tries to pull the node OUT up, while MN2 is trying to pull this node down. This means that there is still a contention between the pull-up and the pull-down devices in the high-to-low transition of the input signal, leading to increase in the delay and consequently the power consumption of the circuit, especially the power of the next stage.

IV . CONVENTIONAL LEVEL SHIFTER

The conventional level shifter is mentioned below,



In order to reduce the existing contention at the high-to-low transition of the structure shown in Figure, the transition current of IP1 and therefore IP2 must be suppressed when MN2 is pulling down the output node. When the input signal changes from “Low” to “High,” MN1 is turned on and MN4 is turned off. During the transition time in which OUT is not corresponding to the logic level of the input, MN4 will be turned on, because the overdrive voltage of MP3 (i.e., VDDH) is larger than that of MN3 (i.e., VDDL). Therefore, a transition current flows through MN4,MN1, and MP1 (i.e., IP1). This current is mirrored into MP2 (i.e., IP2) and tries to pull up the output node. Finally, when OUT is pulled up, MP3 is turned off and consequently the gate of MN4 is pulled down by MN3 meaning that no static current flows through MN4, MN1, and M P1. It should be noted that in order to minimize the power consumption, the aspect ratio of MP1 is chosen smaller than that of MP2. As for the high-to-low transition of the input signal, MN2 is turned on trying to pull down the output node. At the same time, MN1 is turned off meaning that, in contrast to the structure shown in Figure, roughly no transition current flows through MP1 (i.e., IP1 ≈ 0) reducing the strength of MP2 when MN2 is pulling down the output node. However, it should be noted that the node QA is pulled up just to VDDH −|Vth|, whereVth is the threshold voltage of MP1.

V . PROPOSED VOLTAGE LEVELSHIFTER

The proposed level shifter contains three nodes and auxiliary circuits which is able to convert the low input voltages.the circuit also contains the buffer circuit.buffer circuit is used to regenerate the input voltage . When the input changes from “High” to “Low,” MN1 turns off and MN2 turns on trying to pull the node OUT down. As the node OUT is gradually pulled down, MP3 is turned on trying to charge the node QB, which is already discharged to the ground, meaning that a transition current (i.e., IP1) flows through MP1 and MP3 to charge node QB. This current is mirrored to MP2 (i.e., IP2) and therefore tries to pull the node OUT up, while MN2 is trying to pull this node down. This means that there is still a contention between the pull-up and the pull-down devices in the high-to-low transition of the input signal, leading to increase in the delay and consequently the power consumption of the circuit, especially the power of the next stage.

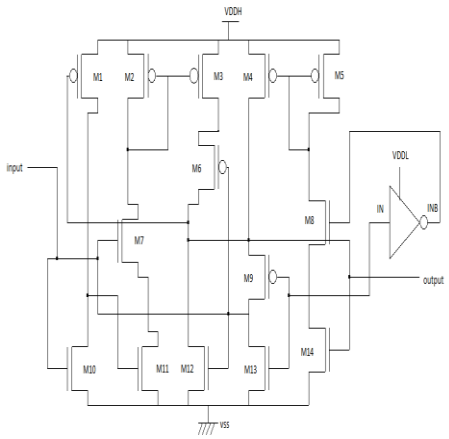


Fig. Schematic of the proposed level shifter.

In order to reduce the existing contention at the high-to-low transition of existing system, the transition current of IP1 and therefore IP2 must be suppressed when MN2 is pulling down the output node. For this purpose, the structure shown in Figure is proposed. The operation of the proposed circuit, is as follows. When the input signal changes from "Low" to "High," MN1 is turned on and MN4 is turned off. During the transition time in which OUT is not corresponding to the logic level of the input, MN4 will be turned on, because the overdrive voltage of MP3 (i.e., VDDH) is larger than that of MN3 (i.e., VDDL). Therefore, a transition current flows through MN4,MN1, and MP1 (i.e., IP1). This current is mirrored into MP2 (i.e., IP2) and tries to pull up the output node. Finally, when OUT is pulled up, MP3 is turned off and consequently the gate of MN4 is pulled down by MN3 meaning that no static current flows through MN4, MN1, and M P1. It should be noted that in order to minimize the power consumption, the aspect ratio of MP1 is chosen smaller than that of MP2. As for the high-to-low transition of the input signal, MN2 is turned on trying to pull down the output node. At the same time, MN1 is turned off meaning that, in contrast to the structure of existing system, roughly no transition current flows through MP1 (i.e., IP1 ≈ 0) reducing the strength of MP2 when MN2 is pulling down the output node. For more details, when MN2 is pulling down the output node, the gate of MP4 is "High" with the value of VDDL and therefore the drain–source voltage of MP2 is decreased. As a result, shown in proposed system the propagation delay and therefore the proposed system Simulated waveforms of the level-shifter structures for low-to-high and high-to-low transitions of the input signal. It should be noted that if the gates of MN2 and MP4 are driven with a voltage higher than VDDL, not only the current of the pull-up device (i.e., IP2) is drastically reduced, but also the strength of the pull-down device (i.e., MN2) is increased. Thus, the contention and therefore the delay and the power (especially the power consumption of the next stage) are significantly reduced. Moreover, the level shifter will be able to operate correctly even for subthreshold input voltages. In order to apply this technique to the proposed structure, as shown in proposed system, an auxiliary circuit (i.e., MP5,MP6,MP7,MN5,MN6, and MN7) is used. This auxiliary circuit turns on only in the high-to-low transition of the input signal to pull up the node QC to a value larger than VDDL. The operation of this part of the circuit is as follows. When IN changes from "High" to "Low" and OUT is not still corresponding to the input logic level, MN6,MN7, and M P6 are turned on and MN5 is turned off. Therefore, a transition current flows through MN6, MN7,MP6, and mirrors to MP7 (i.e., IP7) pulling up the node QC.

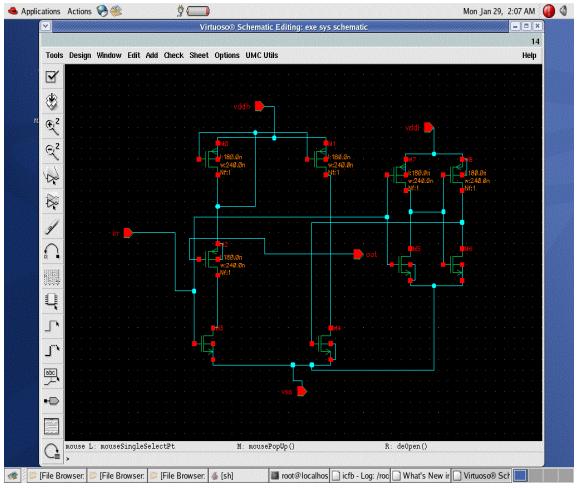


Fig.1.schematic view of level shifter with dynamic current mirror

SIMULATION RESULTS

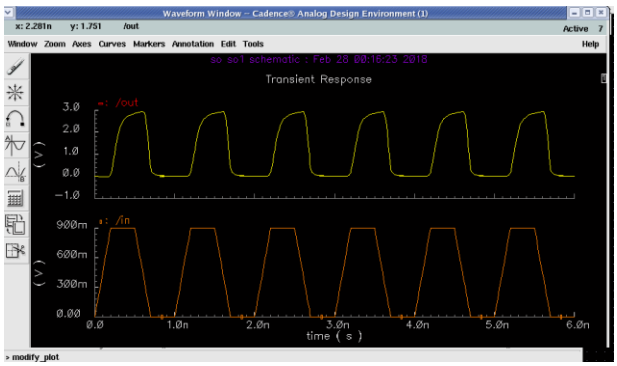


Fig.1.simulation result of level shifter with dynamic current mirror

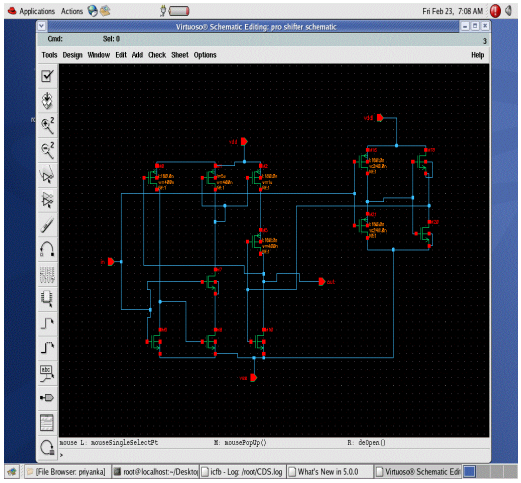


Fig.1.schematic view of conventional level shifter

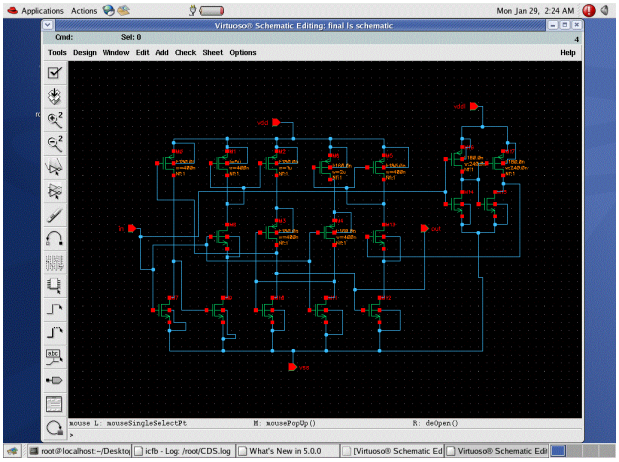


Fig.1.schematic view of proposed level shifter

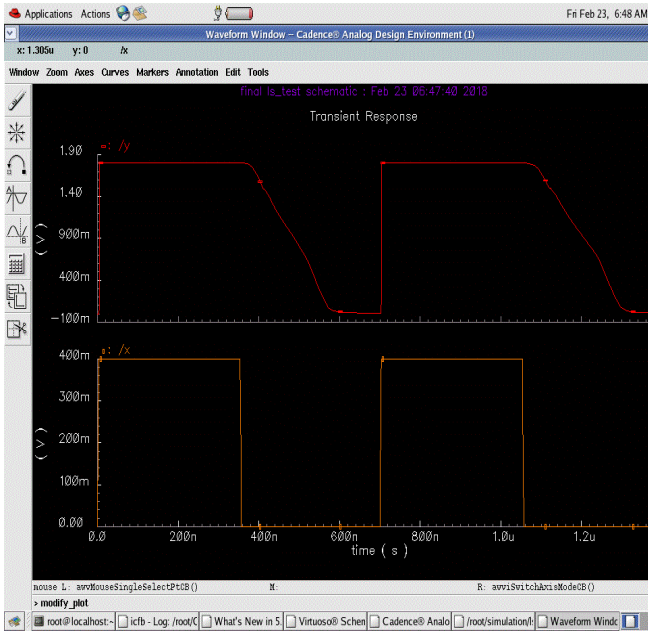


Fig.1.simulation result of conventional level shifter

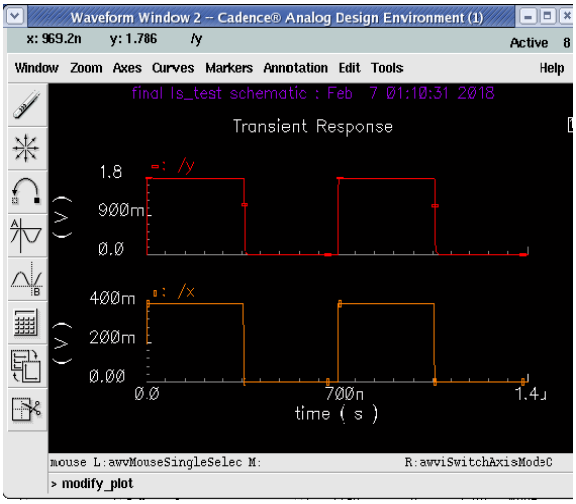


Fig.1.simulation result of proposed level shifter

VI. CONCLUSION

In this brief, a fast and low-power voltage level-shifting architecture was proposed which is able to convert extremely low-input voltages. The efficiency of the proposed circuit is due to the fact that not only the current of the pull-up device is significantly reduced when the pull-down device is pulling down the output node, but the strength of the pull-down device is also increased. Simulation results verified from the power consumption viewpoint.

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